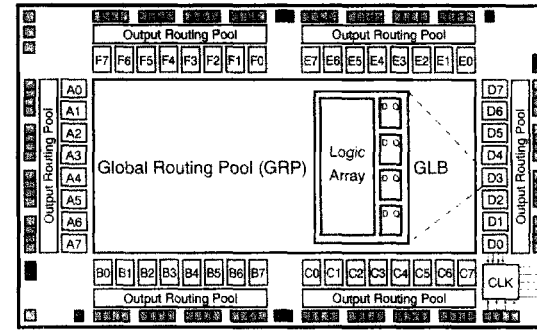
ispLSI® 1048E

High Density Programmable Logic

Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **8,000 PLD Gates**
  - **96 I/O Pins, Twelve Dedicated Inputs**
  - **288 Registers**
  - **High-Speed Global Interconnects**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**
  - **Functionally and Pin-out Compatible to ispLSI 1048C**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **fmax = 125 MHz Maximum Operating Frequency**
  - **tpd = 7.5 ns Propagation Delay**
  - **TTL Compatible Inputs and Outputs**
  - **Electrically Eraseable and Reprogrammable**
  - **Non-Volatile**
  - ***100% Tested at Time of Manufacture***
- **IN-SYSTEM PROGRAMMABLE**
  - **In-System Programmable (ISP™) 5V Only**
  - **Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **Enhanced Pin Locking Capability**
  - **Four Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **Superior Quality of Results**
  - **Tightly Integrated with Leading CAE Vendor Tools**
  - **Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **PC and UNIX Platforms**

Functional Block Diagram



Description

The ispLSI 1048E is a High Density Programmable Logic Device containing 288 Registers, 96 Universal I/O pins, 12 Dedicated Input pins, four Dedicated Clock Input pins, two dedicated Global OE input pins, and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1048E features 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 1048E offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. A functional superset of the ispLSI 1048 architecture, the ispLSI 1048E device adds two new global output enable pins and two additional dedicated inputs.

The basic unit of logic on the ispLSI 1048E device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1...F7 (see Figure 1). There are a total of 48 GLBs in the ispLSI 1048E device. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

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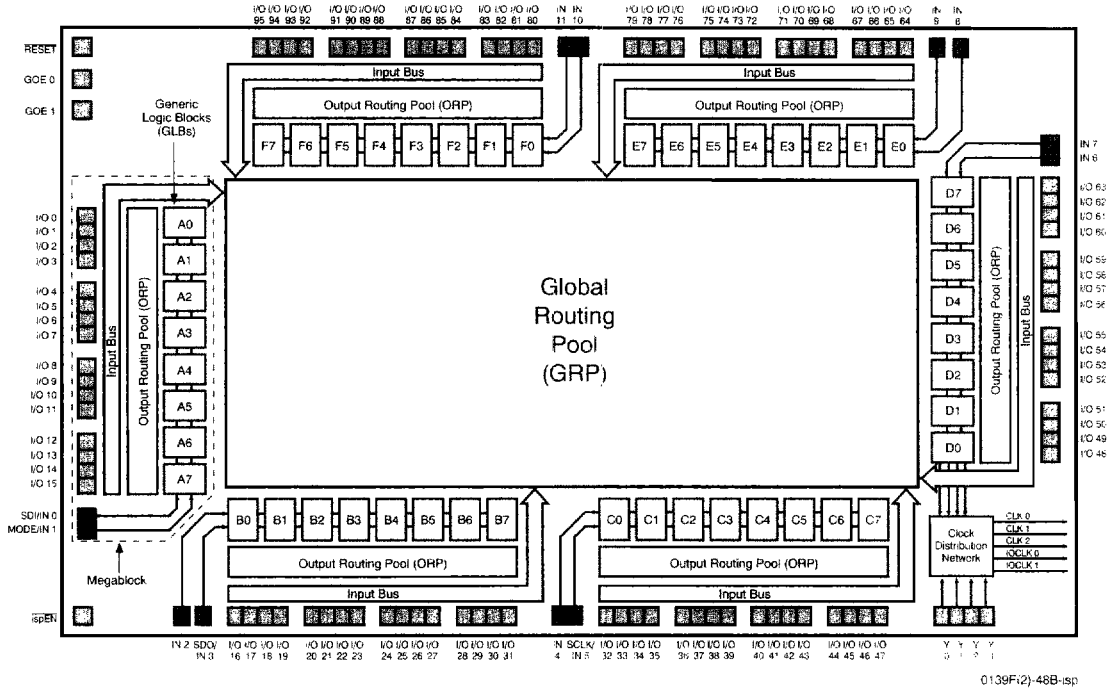
Functional Block Diagram

Figure 1. ispLSI 1048E Functional Block Diagram



The device also has 96 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 16 I/O cells, two dedicated inputs and one ORP are connected together to make a Megablock (see figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each ispLSI 1048E device contains six Megablocks.

The GRP has, as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 1048E device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (D0). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-125		-100		-90		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	7.5	–	10.0	–	10.0	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	10.0	–	12.5	–	12.5	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	125.0	–	100.0	–	90.9	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	91.0	–	71.0	–	71.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle $\left(\frac{1}{t_{wh} + t_{wl}}\right)$	167.0	–	125.0	–	125.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock,4 PT Bypass	5.5	–	6.5	–	6.5	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	4.5	–	6.5	–	6.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	6.5	–	7.5	–	7.5	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	5.5	–	7.5	–	7.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	10.0	–	13.5	–	13.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	5.0	–	6.5	–	6.5	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	12.0	–	15.0	–	15.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	12.0	–	15.0	–	15.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	7.0	–	9.0	–	9.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	7.0	–	9.0	–	9.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	3.0	–	4.0	–	4.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	3.0	–	4.0	–	4.0	–	ns
t_{su3}	–	20	I/O Reg. Setup Time before Ext. Sync Clock (Y2, Y3)	3.0	–	3.5	–	4.0	–	ns
t_{h3}	–	21	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	0.0	–	0.0	–	0.0	–	ns

Table 2-0030A/1048E

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	15.0	–	20.0	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	18.5	–	24.5	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	70.0	–	50.0	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	56.0	–	42.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle $\left(\frac{1}{t_{wh} + t_{wl}}\right)$	100.0	–	77.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock,4 PT Bypass	9.0	–	12.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	7.0	–	9.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	11.0	–	14.5	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	9.0	–	12.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	15.0	–	20.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10.0	–	13.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	18.0	–	24.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	18.0	–	24.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	12.0	–	16.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	12.0	–	16.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	5.0	–	6.5	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	5.0	–	6.5	–	ns
t_{su3}	–	20	I/O Reg. Setup Time before Ext. Sync Clock (Y2, Y3)	4.0	–	6.5	–	ns
t_{h3}	–	21	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	0.0	–	0.0	–	ns

Table 2-0030B/1048E

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.